

Amendments to the Claims:

Please amend claims 1, 9, 10, 16, 23, 29-32, 34, 35, and 37 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being ~~processed by~~ simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit comprises:

a comparator connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between an external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving the external power voltage and generating the internal voltage in response to the driving signal.

2. (Previously Presented) The device of claim 1, wherein the driving signal control circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

3. (Previously Presented) The device of claim 1, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

4. - 6. (Canceled)

7. (Previously Presented) The device of claim 1, wherein the control signal generating circuit comprises a fuse to generate the control signal responsive to the input signal.

8. (Previously Presented) The device of claim 1, wherein the control signal generating circuit comprises an external pad to generate the control signal responsive to the input signal.

9. (Currently Amended) The device of claim 1, wherein the control signal generating circuit comprises a mode setting circuit that sets a mode of the semiconductor device, and generates the control signal in response to the input signal, wherein the input signal is a mode

setting signal comprising a plurality of mode setting bits.

10. (Currently Amended) A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being ~~processed by~~ simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal;

a switching circuit coupled to both the control signal generating circuit and an output of the comparing circuit for receiving the control signal and for transmitting the comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated;

a driving signal control circuit inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

11. (Previously Presented) The device of claim 10, wherein the driving signal control

circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

12. (Previously Presented) The device of claim 10, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

13. (Canceled)

14. (Previously Presented) The device of claim 10, wherein the control signal generating circuit comprises a fuse to generate the control signal responsive to the input signal.

15. (Previously Presented) The device of claim 10, wherein the control signal generating circuit comprises an external pad to generate the control signal responsive to the input signal.

16. (Currently Amended) The device of claim 10, wherein the control signal generating circuit comprises a mode setting circuit that sets a mode of the semiconductor device, and generates the control signal in response to the input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits.

17. (Withdrawn) An internal voltage generating circuit of a semiconductor device,

comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a first internal voltage generating circuit for receiving a reference voltage and an internal voltage to turn the internal voltage to a reference voltage level;

a second internal voltage generating circuit for receiving an external power voltage to turn the internal voltage to an external power voltage level;

a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and

a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

18. (Withdrawn) The circuit of claim 17, wherein the first switching circuit includes a CMOS transmission gate which supplies the external power voltage to the first internal voltage generating circuit when the control signal is inactivated.

19. (Withdrawn) The circuit of claim 17, wherein the switching circuit includes a CMOS transmission gate which supplies the external power voltage to the second internal voltage generating circuit when the control signal is inactivated.

20. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

21. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

22. (Withdrawn) The circuit of claim 17, wherein the control signal generating circuit

activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.

23. (Currently Amended) A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being ~~processed by~~ simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being processed by simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit that cuts off an external power voltage applied to the internal voltage generating circuit when the control signal is activated, a second switching circuit that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal is activated, and a third switching circuit including a CMOS transmission gate which transmits the driving signal when the control signal is inactivated.

24. (Canceled)

25. (Previously Presented) The device of claim 23, wherein the internal voltage

generating circuit includes:

- a comparing circuit for comparing the reference voltage to the internal voltage to generate a comparing signal;
- the third switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated;
- a driving signal control circuit for inactivating the driving signal when the control signal is activated; and
- an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

26. (Withdrawn) The circuit of claim 23, wherein the second internal voltage generating circuit:

- a first internal voltage generating circuit for receiving the second reference voltage and the second internal voltage to turn the second internal voltage to a second reference voltage level;
- a second internal voltage generating circuit for receiving an external power voltage to turn the second internal voltage to an external power voltage level;
- a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and
- a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

27. (Previously Presented) The device of claim 23, wherein the control signal generating circuit comprises a fuse to generate the control signal responsive to the input signal.

28. (Previously Presented) The device of claim 23, wherein the control signal generating circuit comprises an external pad to generate the control signal responsive to the input

signal.

29. (Currently Amended) The device of claim 23, wherein the control signal generating circuit comprises a mode setting circuit that sets a mode of the semiconductor device, and generates the control signal in response to the input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits.

30. (Currently Amended) The device of claim 9, wherein the mode setting circuit produces a value that is represented by the mode setting bits and a mode setting command, wherein the control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.

31. (Currently Amended) The device of claim 16, wherein the mode setting circuit produces a value that is represented by the mode setting bits and a mode setting command, wherein the control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.

32. (Currently Amended) The device of claim 29, wherein the mode setting circuit produces a value that is represented by the mode setting bits and a mode setting command, wherein the control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by the semiconductor device.

33. (Previously Presented) A semiconductor device, comprising:
a control signal generating circuit for generating a control signal responsive to an input

signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit comprises:

a comparator connected between a first node and a second node and comparing the reference voltage to the internal voltage to generate the driving signal;

a first switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated; and

a second switching circuit connected between the second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

34. (Currently Amended) A semiconductor device, comprising:

a control signal generating circuit for generating a control signal responsive to an input signal related to a number of data bits being ~~processed by~~ simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being ~~processed by~~

simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being ~~processed by~~ simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits; and

an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, the internal voltage generating circuit comprising:

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit comprises:

a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

35. (Currently Amended) An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes:

a comparator connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

36. (Previously Presented) An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes:

a comparator connected between a first node and a second node and comparing the reference voltage to the internal voltage to generate the driving signal;

a first switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated; and

a second switching circuit connected between the second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating

the internal voltage in response to the driving signal.

37. (Currently Amended) An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes:

a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

38. (Previously Presented) An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal;

a switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate

which transmits the comparing signal as the driving signal when the control signal is inactivated;
a driving signal control circuit for inactivating the driving signal when the control signal is activated; and
an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

39. (Previously Presented) The device of claim 1, wherein the control signal is activated when the number of data bits being simultaneously input or output by the device is more than 38 bits.

40. (Previously Presented) The device of claim 1, wherein the control signal is inactivated when the number of data bits being simultaneously input or output by the device is less than 18 bits.

41. (Previously Presented) The device of claim 10, wherein the control signal is activated when the number of data bits being simultaneously input or output by the device is more than 38 bits.

42. (Previously Presented) The device of claim 10, wherein the control signal is inactivated when the number of data bits being simultaneously input or output by the device is less than 18 bits.

43. (Previously Presented) The device of claim 23, wherein the control signal is activated when the number of data bits being simultaneously input or output by the device is more than 38 bits.

44. (Previously Presented) The device of claim 23, wherein the control signal is inactivated when the number of data bits being simultaneously input or output by the device is less than 18 bits.